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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,670	08/29/2003	Takuma Hara	241984US2	7771

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,670	HARA ET AL.	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-15* is/are allowed.

6)☒ Claim(s) *1-4,7,16 and 17* is/are rejected.

7)☒ Claim(s) *5,6 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *August 29, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on August 29, 2003.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Thapar (United States Patent 6,580,123).

With respect to independent claim 1, Thapar discloses (see the entire patent, including the Fig. 1A disclosure) a semiconductor device comprising: a first main electrode 24; a second main electrode 25; a semiconductor base region 12 of a first (P) conductivity type; a gate electrode 22 provided in a trench 20 through an insulating film 21, the trench being formed to penetrate the semiconductor base region; and a first semiconductor region 30 of [the] first conductivity type and a second semiconductor region 11 of a second (N) conductivity type provided under the semiconductor base region, a flow of a current between the first and second main electrodes when a voltage of a predetermined direction is applied between these electrodes being controllable in accordance with a voltage applied to the gate electrode, and a depleted region extending from a junction between the first and the second semiconductor regions reaching the trench.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Thapar.

With respect to dependent claim 2, a forward voltage is applied to a p-n junction formed between Thapar's first and second semiconductor regions when the voltage of the predetermined direction is applied between the first and second main electrodes.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Thapar.

With respect to dependent claim 3, Thapar's first semiconductor region 30 is in contact with the trench 20.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Thapar.

With respect to dependent claim 4, a bottom of Thapar's trench 20 is provided within first semiconductor region 30.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Thapar.

Claims 1-4, 7, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa et al. (United States Patent 6,777,746 – hereafter Kitagawa).[1]

With respect to independent claim 1, Kitagawa discloses (see the entire patent, including the Figs. 20-26 disclosure[2]) a semiconductor device comprising: a first main electrode; a second main electrode 10; a semiconductor base region 4 of a first (P) conductivity type; a gate electrode 15 provided in a trench through an insulating film 14, the trench being formed to penetrate the semiconductor base region; and a first semiconductor region 13 of [the] first conductivity type and a second semiconductor region 12 of a second (N) conductivity type provided under the semiconductor base region, a flow of a current between the first and second main electrodes when a voltage of a predetermined direction is applied between these electrodes being controllable in accordance with a voltage applied to the gate electrode, and a depleted region extending from a junction between the first and the second semiconductor regions reaching the trench.

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[1] Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

[2] Kitagawa's Figs. 21-22 are incorrect in that the P-type and N-type drift regions are mislabeled "12" and "13," respectively. Figs. 21-22's P-type and N-type drift regions should be labeled "13" and "12," respectively. See Kitagawa at column 7, lines 24-26, and at Figs. 24-26, for example.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to dependent claim 2, a forward voltage is applied to a p-n junction formed between Kitagawa first and second semiconductor regions when the voltage of the predetermined direction is applied between the first and second main electrodes.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to dependent claim 3, Kitagawa's first semiconductor region 13 is in contact with the trench 20.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to dependent claim 4, a bottom of Kitagawa's trench is provided within first semiconductor region 13 (see Figs. 25-26).

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to dependent claim 7, Kitagawa's device comprises a plurality of the first semiconductor regions 13 and a plurality of the second semiconductor regions 12 arranged alternately on a plane which is substantially perpendicular to a depth direction of the trench.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to independent claim 16, Kitagawa discloses (see the entire patent, including the Figs. 24-26 disclosure) a semiconductor device comprising: a first semiconductor region 7 of a second (N) conductivity type; a semiconductor layer 12/13 provided on the first semiconductor region and having a plurality of second semiconductor regions 13 of a first (P) conductivity type and a plurality of third semiconductor regions 12 of [the] second conductivity type, the second and third semiconductor regions being arranged alternately; a fourth semiconductor region 4 of [the] first conductivity type provided on the semiconductor layer, a fifth semiconductor region 5 of [the] second conductivity type provided on the fourth semiconductor region, a trench penetrating at least the fourth and fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and a gate electrode 15 provided in the trench through an insulating film.

Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

With respect to dependent claim 17, Kitagawa's second and third semiconductor regions are substantially depleted.

Claim 17 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Kitagawa.

Claims 1-4, 7, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira (United States Patent 6,720,615).

With respect to independent claim 1, Fujihira discloses (see the entire patent, including the Figs. 12A-12F disclosure) a semiconductor device comprising: a first main

electrode; a second main electrode; a semiconductor base region 27 of a first (P) conductivity type; a gate electrode 21 provided in a trench through an insulating film 10, the trench being formed to penetrate the semiconductor base region; and a first semiconductor region 2 of [the] first conductivity type and a second semiconductor region 1 of a second (N) conductivity type provided under the semiconductor base region, a flow of a current between the first and second main electrodes when a voltage of a predetermined direction is applied between these electrodes being controllable in accordance with a voltage applied to the gate electrode, and a depleted region extending from a junction between the first and the second semiconductor regions reaching the trench.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to dependent claim 2, a forward voltage is applied to a p-n junction formed between Fujihira first and second semiconductor regions when the voltage of the predetermined direction is applied between the first and second main electrodes.

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to dependent claim 3, Fujihira's first semiconductor region 2 is in contact with the trench (see Fig. 12C).

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to dependent claim 4, a bottom of Fujihira's trench is provided within first semiconductor region 2 (see Fig. 12C).

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to dependent claim 7, Fujihira's device comprises a plurality of the first semiconductor regions 2 and a plurality of the second semiconductor regions 1 arranged alternately on a plane which is substantially perpendicular to a depth direction of the trench (see Figs. 12D-12F).

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to independent claim 16, Fujihira discloses (see the entire patent, including the Figs. 12A-12F disclosure) a semiconductor device comprising: a first semiconductor region 29 of a second (N) conductivity type; a semiconductor layer 1/2 provided on the first semiconductor region and having a plurality of second semiconductor regions 2 of a first (P) conductivity type and a plurality of third semiconductor regions 1 of [the] second conductivity type, the second and third semiconductor regions being arranged alternately; a fourth semiconductor region 27 of [the] first conductivity type provided on the semiconductor layer, a fifth semiconductor region 28 of [the] second conductivity type provided on the fourth semiconductor region, a trench penetrating at least the fourth and fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and a gate electrode 21 provided in the trench through an insulating film 10.

Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

With respect to dependent claim 17, Fujihira's second and third semiconductor regions are substantially depleted.

Claim 17 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Fujihira.

Claims 5, 6 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-15 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable semiconductor devices taken as a whole, including the trenched gate.

Hara et al's United States Patent Application Publication 2004/0094798 is related to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner